ABSTRACT OF THE DISCLOSURE

This invention provides a low level code translation technique that separates a source code into blocks based on a target processor register capability. The source code of a source processor, is first divided into source code blocks based on instruction sequence altering commands such as branch or loop commands. Each of the source code blocks may be further divided into translated code blocks based on the target register capability. A head stub and a tail stub that perform housekeeping tasks are added to each of the translated code block to form translated blocks. The head stubs retrieve source register values from a source register map to initialize target registers and the tail stubs store values of the target registers into the source register map so that the register map contains the most current values of the source registers.